REMARKS

Claims 1-4 were rejected under 35 U.S.C. 102(b) as being clearly anticipated by Shimizu, et al. (U.S. patent 6,242,898).

In a power supply circuit according to the present invention, both the output circuit (23) and the current generation circuit (124) are controlled by the voltage delayed by the delay circuit (22). More specifically, in a power supply circuit according to the present invention,

the output circuit (23) generates the supply voltage from the input constant voltage delayed by the delay circuit (22) and supplies the supply voltage to the load (12), and

the current generation circuit (124) generates a current based on the voltage delayed by the delay circuit (22) and supplies the generated current to the output circuit (23) as a drive current.

The Shimizu reference discloses a delay circuit (D101) and an output circuit (considered to be T104, though not specifically indicated by the Examiner). However, in the Shimizu reference, it is only the output circuit (T104) to which the output of the delay circuit (D101) is directly supplied.

Thus, the Shimizu reference neither discloses nor teaches that a current generation circuit generates a current based on a voltage delayed by a delay circuit.

In the "Office Action Summary", the item 10) remains blank. Please approve the drawings.

Reconsideration and allowance are, therefore, requested.

Respectfully submitted,

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